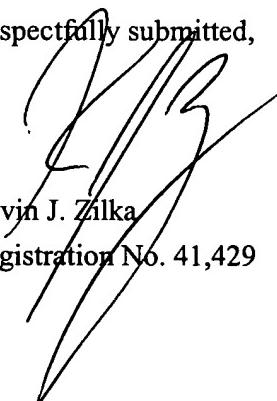


REMARKS

Additional claims have been added which reflect what was set forth in the originally filed application. Further, the specification has been amended to conform with the figures, as originally filed. No new matter has been added.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100.

Respectfully submitted,


Kevin J. Zilka
Registration No. 41,429

P.O. Box 721120
San Jose, CA 95172-1120
Telephone: (408) 505-5100

LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR
METHOD AND APPARATUS FOR A LIGHTING MODULE IN A
GRAPHICS PROCESSOR

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 JC971 U.S. PTO
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5 RELATED APPLICATIONS

The present application is related to applications entitled "Method,

10 The present application is related to applications entitled "Method, Apparatus and Article of Manufacture for Area Rasterization using Sense Points and Article of Manufacture for Area Rasterization using Sense Points" which was filed on December 06, 1999 under serial number 09/455,305, and attorney docket number NVIDP005, "Method, Apparatus and Article of Manufacture for Boustrophedonic Rasterization" which was filed under attorney and Article of Manufacture for Boustrophedonic Rasterization" which was docket number NVIDP006, "Method, Apparatus and Article of Manufacture for filed on December 06, 1999 under serial number 09/454,505 and attorney Clip-less Rasterization using Line Equation-based Traversal" which was filed under docket number NVIDP007, "Method, Apparatus and Article of Manufacture attorney docket number NVIDP007, "A Transform, Lighting and Rasterization for Clip-less Rasterization using Line Equation-based Traversal" which was System Embodied on a Single Semiconductor Platform" which was filed under filed on December 06, 1999 under serial number 09/455,728, and attorney attorney docket number NVIDP008, "Method, Apparatus and Article of Manufacture docket number NVIDP007, "Method, Apparatus and Article of Manufacture for a Vertex Attribute Buffer in a Graphics Processor" which was filed under for Transform, Lighting and Rasterization on a Single Semiconductor attorney docket number NVIDP009, "Method, Apparatus and Article of Manufacture Platform" which was filed on December 06, 1999 under serial number for a Transform Module in a Graphics Processor" which was filed under attorney 09/454,510, and attorney docket number NVIDP008, "Method, Apparatus docket number NVIDP010, and "Method, Apparatus and Article of Manufacture for and Article of Manufacture for a Vertex Attribute Buffer in a Graphics 20 a Sequencer in a Transform/Lighting Module Capable of Processing Multiple Processor" which was filed on December 06, 1999 under serial number Independent Execution Threads" which was filed under attorney docket number 09/454,525, and attorney docket number NVIDP009, "Method, Apparatus NVIDP012 which were filed concurrently herewith, and which are all incorporated and Article of Manufacture for a Transform Module in a Graphics Processor" herein by reference in their entirety.

25 which was filed on December 06, 1999 under serial number 09/456,102 and attorney docket number NVIDP010, and "Method, Apparatus and Article of Manufacture for a sequencer in a Transform/Lighting Module capable of Processing Multiple Independent Execution Threads" which was filed on December 06, 1999 under FIELD OF THE INVENTION serial number 09/456,104, and attorney docket number NVIDP012 which were filed concurrently herewith, and which are all incorporated herein by reference in their entirety.

The present invention relates generally to graphics processors and, more particularly, to a lighting module of a graphics pipeline system.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects and advantages are better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

- 5 ~~Figure 1 illustrates the prior art;~~
 ~~Figure 1 illustrates a prior art method of rasterization;~~
- 10 ~~Figure 1A is a flow diagram illustrating the various components of one embodiment of the present invention implemented on a single semiconductor platform;~~
- 15 ~~Figure 1B is a flow diagram illustrating the various components of one embodiment of the present invention implemented on a single semiconductor platform;~~
- 20 Figure 2 is a schematic diagram of a vertex attribute buffer (VAB) in accordance with one embodiment of the present invention;
- 25 Figure 2A is a chart illustrating the various commands that may be received by VAB in accordance with one embodiment of the present invention;
- 30 Figure 2B is a flow chart illustrating a method of loading and draining vertex attributes to and from VAB in accordance with one embodiment of the present invention;
- 35 Figure 2C is a schematic diagram illustrating the architecture of the present invention employed to implement the operations of Figure 2B;
- 40 Figure 3 illustrates the mode bits associated with VAB in accordance with one embodiment of the present invention;

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 illustrates the prior art. Figures 1A - 32C show a graphics pipeline system of the present invention.

5 Figures 1 and 1A show the prior art. Figures 1B - 32C show a graphics pipeline system of the present invention.

Figure 1A is a flow diagram illustrating the various components of one embodiment of the present invention. As shown, the present invention is divided into four main modules including a vertex attribute buffer (VAB) 50, into four main modules including a vertex attribute buffer (VAB) 50, a transform module 52, a lighting module 54, and a rasterization module 56 with a set-up module 57. In one embodiment, each of the foregoing modules 57. In one embodiment, each of the foregoing modules is situated on a single semiconductor platform in a manner that will be described hereinafter in greater detail. In the present description, the single semiconductor platform may refer to a sole unitary semiconductor-based integrated circuit or chip.

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The VAB 50 is included for gathering and maintaining a plurality of vertex attribute states such as position, normal, colors, texture coordinates, etc. Completed vertices are processed by the transform module 52 and then sent to the lighting module 54. The transform module 52 generates vectors for the lighting module 54 to light. The output of the lighting module 54 is screen space data suitable for the set-up module which, in turn, sets up primitives. Thereafter, rasterization module 56 carries out rasterization of the primitives. It should be noted that the transform and lighting modules 52 and 54 might only stall on the command level such that a command is always finished once started.

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In one embodiment, the present invention includes a hardware implementation that at least partially employs Open Graphics Library (OpenGL[®]) and D3DTM transform and lighting pipelines. OpenGL[®] is the computer industry's standard application program interface (API) for defining 2-D and 3-D graphic images. With OpenGL[®], an application can create the same effects in any operating system using any OpenGL[®]-adhering graphics adapter. OpenGL[®] specifies a set of